Overview and Applications

The National Instruments PXI-665x timing and synchronization control modules use the trigger bus, star trigger, and system reference clock features of PXI to implement advanced multidevice or multichassis synchronization. You can vastly improve the accuracy of measurements, implement advanced triggering schemes, or synchronize multiple devices and/or multiple chassis to act as a single system for high-channel-count applications.

### NI PXI-665x

- Works with all PXI modules
- Multichassis PXI synchronization
- Onboard routing of internal or external clock and trigger signals
- PXI slot 2 star trigger controller
- Onboard high-stability references
  - OCXO, 50 ppb (6653)
  - TCXO, 1 ppm (6652)
- Reference clock import and export with PLL capabilities
- DC to 105 MHz, 1 µHz resolution DDS clock generation
- Software trigger generation
- Frequency measurement capabilities
- LabVIEW FPGA targets (PXI-6653, PXI-6652)

### Operating Systems
- Windows 2000/XP
- LabVIEW Real-Time

### Recommended Software
- LabVIEW
- LabWindows/CVI

### Driver Software (included)
- NI-SYNC

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**Table 1. NI PXI-665x Features**

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<td>CLK10 in</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>CLK10 out</td>
<td>–</td>
<td>–</td>
<td>–</td>
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<tr>
<td>General-purpose PFI lines</td>
<td>2 SMB</td>
<td>6 SMB</td>
<td>6 SMB</td>
</tr>
<tr>
<td>Programmable voltage threshold</td>
<td>–</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Trigger Routing</td>
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<tr>
<td>Star trigger source (PXI_STAR)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PXI trigger bus (PXI_TRIG)</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<tr>
<td>Onboard Clock Sources</td>
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<td>TCXO (1 ppm)</td>
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<td>DC to 105 MHz</td>
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Figure 1. Block Diagram of PXI-6652 and PXI-6653 Master Modules
PXI Timing and Synchronization Control

PXI-665x modules provide full control of the following timing and synchronization features of the PXI backplane. To act as a PXI star trigger controller or to provide a high-accuracy 10 MHz reference clock, the PXI-665x module must be installed in slot 2 of the PXI chassis, as shown below in Figure 3.

- **Star trigger (PXI_STAR)** – 13 equal-trace-length, point-to-point lines for providing low-skew (<1 ns) trigger or clock signals from slot 2 to slots 3 through 15.
- **Trigger bus (PXI_TRIG)** – 8 bused TTL lines for general-purpose routing of triggers, clocks, and handshaking signals.
- **10 MHz clock (PXI_CLK10)** – capable devices, such as the NI PXI-5xxx modular instruments, can phase-lock to the high-accuracy, low-jitter 10 MHz reference clock for improved accuracy.

**High-Stability 10 MHz Time Base**

When installed in slot 2 of a PXI chassis, the PXI-6652 and PXI-6653 modules can override the built-in 10 MHz reference clock on a PXI chassis. Typically, most PXI chassis provide a 10 MHz reference clock with 25 ppm accuracy (10 MHz ±250 Hz). This accuracy is improved to 1 ppm with the PXI-6652, and to 50 ppb with the PXI-6653. Many modules, such as the PXI-5xxx modular instruments, have phase-lock-loop (PLL) circuitry to synchronize with the 10 MHz reference clock.

**High-Resolution DDS Clock**

The onboard direct digital synthesis (DDS) clock of the PXI-6652 and PXI-6653 modules provides an extremely high-resolution programmable clock source that can generate clocks from DC to 105 MHz in frequency with 1 µHz resolution. Use this clock as a common time base for data acquisition modules. For example, the DDS clock can be used to provide a 13.1 MHz oversampling clock for synchronization of multiple NI PXI-4472 dynamic signal acquisition modules.

**NI-SYNC Software**

NI-SYNC driver software, included free, provides powerful yet easy-to-use control of PXI-665x modules. NI-SYNC includes many examples for synchronizing of data acquisition modules, arbitrary waveform generators, digitizers, and dynamic signal acquisition (DSA) modules in both LabVIEW and LabWindows/CVI.

**LabVIEW FPGA Module**

The LabVIEW FPGA Module provides LabVIEW developers with the ability to define their own hardware by targeting their LabVIEW block diagrams to the FPGAs on supported National Instruments hardware. The LabVIEW FPGA Module can target the FPGA on the PXI-6652 and PXI-6653 modules to develop custom, user-defined applications.

**Multichassis Synchronization**

Using a combination of master PXI-6652 and PXI-6653 modules, in conjunction with slave PXI-6651 modules, multiple PXI chassis can be tightly synchronized. Each master module can synchronize up to three slave modules. With these modules, you can create very high-channel-count synchronized data acquisition systems.
PXI Timing and Synchronization Control

Figure 5. In this example, three PXI chassis containing 13 PXI-4472 8-channel 102.4 kS/s simultaneous-sampling dynamic signal acquisition modules are synchronized. The result is a 312-channel synchronized acquisition system.

**Specifications**

**CLKIN Input Characteristics**
- **Fundamental frequency range**: 1 MHz to 105 MHz sine or square
- **Input impedance**: 50 Ω, nominal
- **Input coupling**: AC
- **Voltage range**: 400 mVpp to 5 Vpp
- **Absolute maximum input voltage**: 6 Vpp
- **CLKIN to PXI_CLK_IN delay**
  - Uncompensated: 14 ns to 14.7 ns, typical
  - PLL compensated: ±1 ns, maximum
- **PLL frequency accuracy requirement**
  - PLL and OCXO (PXI-6653): ±1.5 ppm
  - PLL and TCXO (PXI-6652): ±5 ppm
  - Replacing PXI_CLK10: ±100 ppm
- **Jitter added to CLKIN**
  - Without PLL: 0.5 ps rms, 10 Hz to 100 kHz
  - With PLL: 0.6 ps rms, 10 Hz to 100 kHz
- **Duty cycle distortion of CLKIN**
  - To PXI_CLK10 without PLL: ±1%, maximum
  - Required input duty cycle when using PLL: 45 to 55%

**CLKOUT Output Characteristics**
- **Output frequency**
  - From PXI_CLK10: 10 MHz
  - From OCXO (PXI-6653): 10 MHz
  - From TCXO (PXI-6652): 10 MHz
  - From DDS (PXI-6652/6653): 1 Hz to 105 MHz
- **Duty cycle**: 40 to 60%
- **Output impedance**: 50 Ω, nominal
- **Output coupling**: AC
- **Clock amplitude software configurable to two voltage levels (low and high drive)**
  - Open load, low drive: 2.0 Vpp
  - Open load, high drive: 5.0 Vpp
  - 50 Ω load, low drive: 1.0 Vpp
  - 50 Ω load, high drive: 2.5 Vpp
- **Clock rise/fall time (10 to 90%)**
  - Low drive: 0.5 ns, 2.5 ns max
  - High drive: 0.5 ns, 2.5 ns max

**PFI <0…5> Input Characteristics**
- **Frequency range**: DC to 105 MHz
- **Input impedance**: 50 Ω, nominal, or 1 kΩ
- **Input coupling**: DC
- **Voltage level**: 0 to 5 V
- **Absolute maximum input voltage**: ±5.25 V, max
- **Input threshold**
  - Voltage level: 0 to 4.3 V, software-selectable
  - Voltage resolution: 16.8 mV (8 bit)
  - Error: ±50 mV
- **Asynchronous delay tpd**
  - PFI <5…0> to PXI_TRIG<0…7>: 15 to 23 ns, typical
  - PFI <5…0> to PXI_STAR<0…12>: 10 to 19 ns, typical
  - Synchronized trigger input setup time: 11.2 ns, typical relative to PXI_CLK10
  - Synchronized trigger input hold time: -10.8 ns, typical relative to PXI_CLK10

**Ordering Information**
- NI PXI-6653 (Master, OCXO): 778715-01
- NI PXI-6652 (Master, TCXO): 778726-01
- NI PXI-6651 (Slave): 778725-01

**Cables**
- SMB-210: 188858-01
- Dual SMB Plug to Dual SMB Plug Coax, 50 Ω, 1 m
- SMB-200: 188859-01
- SMB Plug to SMB Plug Coax, 50 Ω, 1 m

**BUY ONLINE!**
For complete product specifications, pricing, and accessory information, call (800) 813-3693 (U.S. only) or go to ni.com/pxi
Specifications

PFI <0…5> Output Characteristics
- Frequency range: DC to 105 MHz
- Output impedance: 50 Ω, nominal
- Output coupling: DC
- Voltage level into 50 Ω: 0 to 1.6 V
- Voltage level into open circuit: 0 to 3.3 V
- Absolute maximum applied voltage: ±5.25 V
- Synchronized trigger clock to output time: 8.4 ns, relative to PXI_CLK10
- Output-to-output skew, synchronous: 500 ps, typical

PXI_STAR Trigger Characteristics
- PXI_STAR<0…12> to PXI_STAR<0…12>: 300 ps, typical output skew at NI PXI-665x backplane connector
- Asynchronous delays, tpd:
  - PXI_STAR<0…12> to PFI<0…5>: 7 to 11 ns, typical
  - PXI_STAR<0…12> to PXI_TRIG<0…7>: 13 to 19 ns, typical

PXI Trigger Characteristics
- PXI_TRIG<0…7> to PXI_TRIG<0…7> output skew: 5 ns, typical
- Asynchronous delay, tpd:
  - PXI_TRIG<0…7> to PFI<0…5>: 11 to 17 ns, typical
  - PXI_TRIG<0…7> to PXI_TRIG<0…7>: 5 ns, typical

OCXO Characteristics (PXI-6653 Only)
- Frequency: 10 MHz
- Warm-up time: 3 minutes
- Initial accuracy: ±3.2 ppb
- Long-term stability: ±50 ppb/year
- Temperature stability:
  - 0 to 40 °C: ±5 ppb
  - 0 to 55 °C: ±10 ppb
- Jitter:
  - to CLKOUT: 2.0 ps
  - to CLK10In: 1.5 ps

TCXO Characteristics (PXI-6652 Only)
- Frequency: 10 MHz
- Initial accuracy: ±2.5 ppm
- Long-term stability:
  - ±1 ppm
- Temperature stability (0 to 55 °C):
  - ±2 ppm

DDS Characteristics
- Frequency range: 1 Hz to 105 MHz
- Frequency resolution: ≤1.1 µHz
- Frequency accuracy: Inherits PXI_CLK10 accuracy

Power Requirements
- +5 V: 2 A, maximum
- +3.3 V: 600 mA, maximum
- +12 V: 500 mA, maximum
- -12 V: 0 A, maximum

Physical
- Dimensions (1 slot, 3U): 10 by 16 cm (3.9 by 6.3 in.)
- Install in PXI Slot 2 for full functionality
- Front panel connectors: SMB male, 50 Ω
- Front panel indicators: 2 tricolor LEDs
- Maximum cable length, direct connections (no splitter):
  - PFI/CLKOUT, DC to 10 MHz: 200 m
  - CLKOUT high gain, 105 MHz: 100 m
  - PFI/CLKOUT low gain, 105 MHz: 30 m

Operating Environment
- Ambient temperature: 0 to 55 °C
- Relative humidity: 10 to 90%, noncondensing
- Maximum altitude: 2000 m (at 25 °C ambient)

Storage Environment
- Ambient temperature: -20 to 70 °C
- Relative humidity: 5 to 95%

Shock and Vibration
- Operational shock: 30 g peak, half-sine, 11 ms pulse
- Random vibration:
  - Operating: 5 to 500 Hz, 0.3 g
  - Nonoperating: 5 to 500 Hz, 2.4 g

Safety
- The product is designed to meet the requirements of the following standards of safety:
  - UL 3111-1
  - IEC 61010-1, EN 61010-1
  - CAN/CSA C22.2 No. 1010.1

Electromagnetic Compatibility
- Emissions: EN 55011 Class A at 10 m
- EMC/EMI: CE, C-Tick, and FCC Part 15 (Class A) Compliant

CE Compliance
- This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:
  - Low voltage directive (safety): 73/23/EEC

Specifications subject to change without notice.
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