

# LabVIEW FPGA Module

## NI LabVIEW FPGA Module

- Graphically develop custom FPGA logic and download to NI reconfigurable I/O (RIO) hardware targets
- Create custom mix of analog I/O, digital I/O, counters, and triggers using off-the-shelf hardware
- Implement custom timing, triggering, and I/O logic with 25 ns resolution
- Define custom control and signal processing algorithms with loop rates up to 40 MHz
- Execute multiple tasks simultaneously with hardware determinism
- Integrate VHDL into your LabVIEW FPGA application

### Required Software

- LabVIEW Full or Professional Development System, current version

### Recommended Software

- LabVIEW Real-Time Module

### NI FPGA Hardware

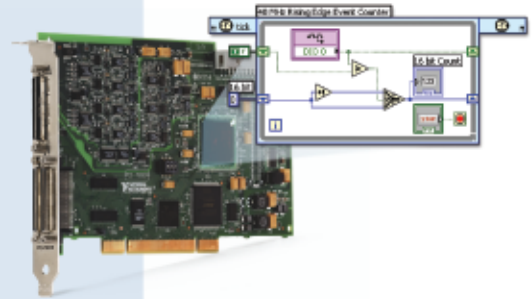
- R Series Reconfigurable I/O
  - PCI-7831R, PXI-7831R
  - PXI-7811R
- Compact vision systems
  - NI CVS 1455
  - NI CVS 1456
- CompactRIO
  - cRIO-910x chassis

### System Requirements

- Windows 2000/XP
  - 512 MB<sup>1</sup> RAM
  - 2 GB disk space

<sup>1</sup>Future targets may require more RAM

NEW



## Overview

The National Instruments LabVIEW FPGA Module extends the LabVIEW graphical development to field-programmable gate arrays (FPGAs) on NI reconfigurable I/O (RIO) hardware. Using the NI LabVIEW FPGA Module, you can develop intuitive graphical code to define custom I/O and control hardware without prior knowledge of digital design or complex EDA tools. In addition, you can use LabVIEW FPGA and RIO hardware to rapidly prototype and develop FPGA code. LabVIEW graphical programming is an intuitive way to program embedded devices because the block diagram of a LabVIEW FPGA VI resembles flow charts and block diagrams used by many engineers. You can also integrate RIO hardware with a LabVIEW for Windows or LabVIEW Real-Time system.

LabVIEW FPGA and RIO technology are ideal for applications requiring custom hardware. These include a variety of applications such as:

- Integrating custom timing, triggering, and synchronization
- Integrating a custom mix of analog, digital, counters, and triggers onto one device
- Integrating custom digital communication protocols
- Parallel processing
- Custom motion control
- Off-loading signal processing and control from a host PC or real-time system

The LabVIEW FPGA Module targets a growing family of NI RIO devices as shown in Figure 1. Use R Series DAQ devices for complex data acquisition or real-time I/O applications. Develop custom FPGA logic on a compact vision system to add custom triggering, PWM signals, motion control, or custom communications protocols to machine vision applications. Use the CompactRIO platform for

modular FPGA-timed I/O with built-in signal conditioning and direct signal connectivity for maximum flexibility in embedded measurement and control applications.

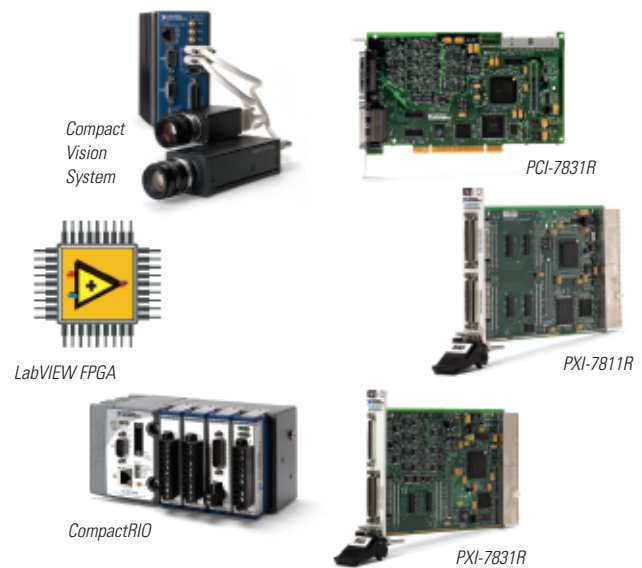


Figure 1. NI Family of LabVIEW FPGA Targets

## Graphical Development Environment

When targeted to the FPGA device, LabVIEW displays a focused palette of functions that can be implemented on the FPGA. Use a combination of these functions to define logic and embed intelligence onto your RIO device.

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The LabVIEW FPGA functions palette includes typical structures and functions such as while loops, for loops, case structures, sequence structures, comparison logic, array and cluster manipulations, occurrences, and timing. In addition, a dedicated set of LabVIEW FPGA-specific functions for math, signal generation and analysis, linear and non-linear control, analog I/O and digital I/O are included.

Figure 2 shows an example of a custom counter and period measurement application developed in LabVIEW and downloaded to a RIO device. The upper loop increments a 16-bit counter for every falling edge from DI 0 (digital line 0 configured for input), makes the count value available for the host application, and generates a digital pulse on DO 1 (digital line 1 configured for output) every four falling edges. The lower loop implements a period measurement by measuring the number of clock cycles between rising edges detected on a digital input line. The resolution of the measurement is determined by the loop rate. The single-cycle timed loop structure that encloses the custom counter and period measurement code iterates every FPGA clock cycle.

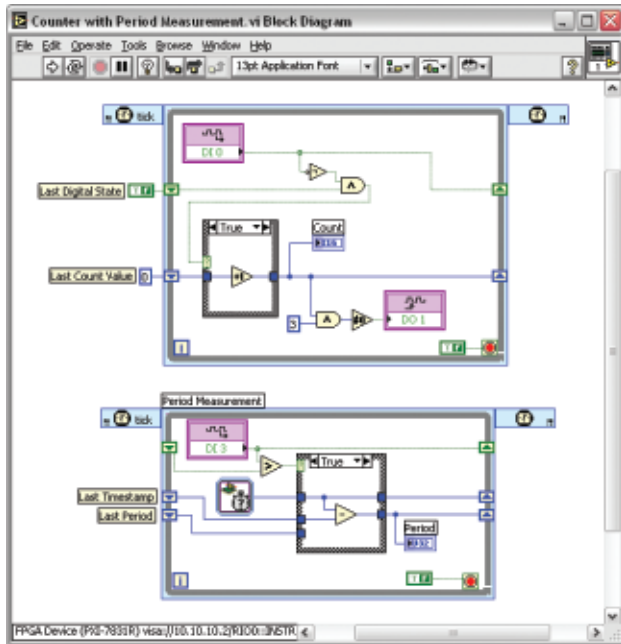


Figure 2. LabVIEW FPGA Block Diagram of a Custom Counter and Period Measurement

Finally, you can integrate existing VHDL IP cores, such as communication protocols or filter cores, into a LabVIEW FPGA block diagram using the HDL interface node.

## Parallel Execution

With the LabVIEW FPGA Module, you can use the parallelism of LabVIEW to create true simultaneous execution in hardware. The compiled code is implemented in hardware by configuring logic cell resources on the FPGA. The embedded VI does not need to access a main processor to execute. Instead, independent sections of code, such as parallel loops, are implemented as independent sections of the chip. After the chip is configured, data is clocked through the device at a rate specified by the onboard clock, executing independent areas of the chip simultaneously. In Figure 2, the loops execute simultaneously without competing for execution time because of the parallel architecture of FPGA hardware.

## Software Structures in Hardware

The graphical block diagram from a LabVIEW FPGA VI is implemented in hardware. The terminals on the left and right side of each loop pass the data value from one loop iteration to the next and represent registered data on the FPGA. Each control and indicator on the front panel, in this case the count and period indicators, are used for communication between the RIO device and host application. Controls and indicators are also represented as registers on the FPGA. Finally, the DI and DO terminals read and write data directly from the FPGA I/O block.

## Debugging Tools

Depending on the complexity of your code and the specifications of your development system, the compile time for an FPGA VI can range from minutes to several hours. To maximize development productivity, the LabVIEW FPGA Module includes an emulation mode for R series targets so you can verify the logic of your design before initiating the compile process. While targeted to the FPGA emulator, LabVIEW accesses I/O from the device and executes the VI logic on the Windows development machine. In this mode, you can use the same debugging tools available in LabVIEW for Windows, such as execution highlighting, probes, and breakpoints.

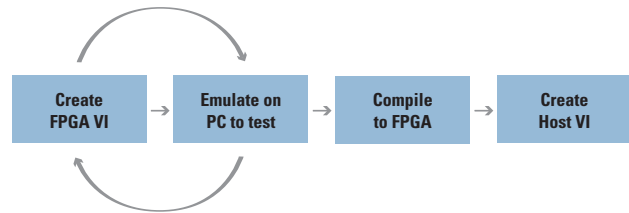


Figure 3. Application Development Flow for LabVIEW FPGA Applications

# LabVIEW FPGA Module

## System Architectures

Once your LabVIEW FPGA code is complete, LabVIEW synthesizes the code to run on the RIO device. Once downloaded to the target, the embedded LabVIEW FPGA VI can execute in one of the following three different configurations:

- Autonomously, where the FPGA device runs independent of a host application.
- Combined with a PC running LabVIEW for Windows, where data is transferred from the FPGA device to the PC for off-line floating-point analysis, networking, file I/O, or display on a graphical user interface.
- Combined with a LabVIEW Real-Time system, where data is transferred from the FPGA device to a real-time target with a dedicated processor running a real-time OS.

The LabVIEW Real-Time system provides a deterministic processing engine for functions performed synchronously or asynchronously to the FPGA. For example, floating-point arithmetic, including FFTs, PID calculations, and custom control algorithms, are often performed in the LabVIEW Real-Time environment. Relevant data can be stored on a LabVIEW Real-Time system or transferred to a LabVIEW for Windows host machine for off-line analysis, data logging, or user interface displays.

## FPGA Host Interface Development

From a LabVIEW Real-Time or LabVIEW for Windows application, you can easily access data using the controls and indicators from your LabVIEW FPGA VI using the FPGA host interface. The FPGA host interface is similar to VI server programming on LabVIEW for Windows. In addition, through the FPGA host interface you can generate interrupts from the LabVIEW FPGA VI and then acknowledge and clear these interrupts from a LabVIEW Real-Time or LabVIEW for Windows application.

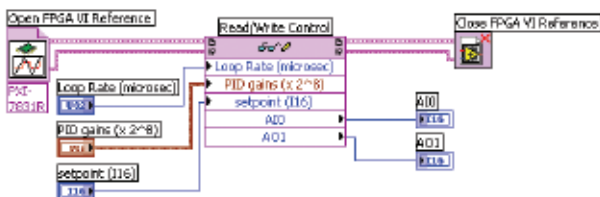
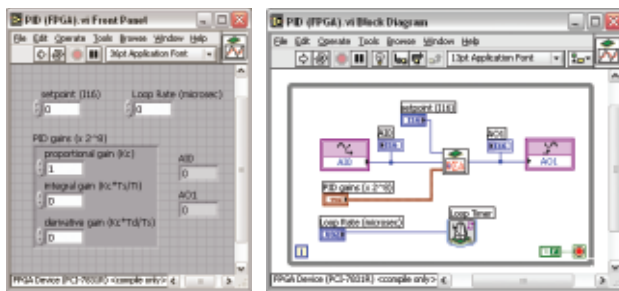


Figure 4. Embedded LabVIEW FPGA VI with Corresponding Host VI

## LabVIEW FPGA Hardware Targets R Series DAQ Devices

NI PCI or PXI R Series plug-in DAQ devices provide analog and digital data acquisition and control for high-performance, user-configurable timing and synchronization, as well as onboard decision-making. With R Series RIO devices and LabVIEW FPGA,



you can extend your PXI or PCI measurement and control system by adding user-defined hardware for operations such as custom discrete and analog control, sensor simulation, digital protocol emulation, and precise custom timing and control.

## CompactRIO

CompactRIO is a small, industrially rugged, modular control and acquisition platform to give you high performance I/O and unprecedented flexibility in system timing. You can use CompactRIO



as signal conditioning for an R Series DAQ device or to build an embedded system for applications such as in-vehicle data acquisition, mobile NVH testing, and embedded machine control systems. Among other industrial certifications and ratings, the CompactRIO system is designed for greater than 50 gs of shock and has a -40 to 70 °C temperature range.

## Compact Vision System

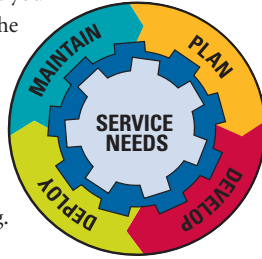


The compact vision system is a rugged machine vision package that withstands the harsh environments common in robotics, automated test, and industrial inspection systems. NI CVS-145x systems offer unprecedented I/O capabilities and network connectivity for distributed machine vision applications.

CVS 145x systems use IEEE 1394 (FireWire) technology, compatible with more than 40 cameras with a wide range of functionality, performance, and price. CVS 1455 and 1456 systems contain a configurable FPGA for implementing custom counters, timing, or motor control into your machine vision application.

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