Wide Range Single- and Multi-Start Time-to-Digital Converter

- 12 channel single-stop time-to-digital converter (TDC) with single-start and multi-start acquisition modes
- 50 ps timing resolution
- Wide range with up to 20 s between first and last events
- Large internal memory buffer, with up to 512 events per channel
- Low jitter (<3 ps rms) high stability (±2 ppm) internal clock source
- External 10 MHz reference input
- FPGA based Data Processing Unit (DPU)
- Fast readout, with DMA mode for increased data throughput
- Overvoltage-protected inputs, with 50 Ω K-Lock (LEMO) connectors
- Built-in self calibration
- Modular, single-slot 6U PXI/CompactPCI
- Low power consumption (<22 W)
Multichannel High-Resolution Time Measurement

The Acqiris TC840 time-to-digital converter (TDC) is designed specifically for use in large scale experiments including particle accelerator timing, nuclear fusion studies, and explosive testing. It is also well suited for use in commercial instrumentation including time-of-flight measurement in mass spectrometry and 3D geological mapping.

The TC840 can be viewed as a free running high-resolution (50 ps) counter with each individual channel capable of recording the time of arrival of trigger signals and storing this data in the local memory. The time base consists of a low phase noise PLL with very low jitter (<3 ps rms) and a stable high-accuracy 10 MHz reference. This time base can also be referenced to an external 10 MHz source through an auxiliary input.

The TC840 is a single- or multi-start, single-stop TDC. It has thirteen identical hardware channels, one common start channel and twelve independent stop channels. The timing information on the twelve independent channels is measured relative to the one common start channel.

Timing Calculation and Fast Data Readout

The timing information of the start and stop events on all 13 channel inputs is obtained by combining a coarse-grain (5 ns) wide-range (32 bits) real-time count with a much finer grained interpolated result coming from the analysis of a ramp signal started by the event.

Each channel consists of a programmable comparator, an XOR gate used to select the active slope, a stable signal generator, and an analog to digital converter (ADC). Once digitized, the data are fed to a Xilinx Virtex-2 Pro FPGA-based Data Processing Unit (DPU) for storage and readout. Data readout is achieved with a fast direct memory access (DMA) mode at up to 100 MB/s.

Each channel is processed to determine the real time of each detected event, start and stop. The final relative time value is obtained by subtracting the start time from each stop time. The large internal memory buffer on the card allows the recording of up to 512 events per channel.

An additional auxiliary input for a common veto signal can be used to enable/disable all start and stop detection, as desired.

Self Calibration

To achieve the desired precision on all of the input channels, the TC840 time-to-digital converter has a powerful self calibration routine.

This self calibration is done simply through a software command available in the driver, so no extra programming is needed.
Wide Range Single- and Multi-Start Time-to-Digital Converter
Model TC840, 12 Channel, 50 ps Resolution

Signal Input

Connectors  
50 Ω K-Lock (LEMO) type

Impedance  
50 Ω ±1%

Threshold  
Programmable from -1.5 V to +1.5 V, in 0.732 mV steps (12-bit)

Sensitivity  
100 mV over threshold for 350 ps (minimum pulse to trigger)
  Hysteresis 15 mV

Channels  
One common start
  Twelve inputs stop

Protection  
Clamping diodes at ±2.5 V, 0.5 W max into 50 Ω

Propagation Delay Skew  
Δtpd = 15 ps for 10 mV to 100 mV,
  Δtpd = 40 ps for 100 mV to 2 V

VSWR (typ.)  
< 1.5 from DC to 1 GHz

VETO IN  
50 Ω input with programmable threshold

REF IN  
50 Ω input for external high-precision 10 MHz source

Time Resolution and Range

Time Resolution  
50 ps

Time Range  
up to 20 s

Integral Nonlinearity  
±50 ps

Differential Nonlinearity  
±30 ps

Post-Start Dead Time  
10 ns

Clock Accuracy  
Better than ±2 ppm

Clock Jitter  
< 3 ps rms

Internal Reference Frequency  
10 MHz

Acquisition and Readout

Acquisition Modes  
Single-start – Single-stop
  Multi-start – Single-stop

Readout Modes  
DMA–100 MB/s

PCI Transfer Speed  
High-speed PCI bus transfers data at sustained rates up to 100 MB/s to host PC

PC System Requirements

Processor  
150 MHz Pentium (or higher)
  Hard Drive Space
  20 MB minimum

Memory  
64 MB RAM (more is recommended when working with several cards with large acquisition memories)

Operating System  
Windows 95/98/NT4/2000/XP
  VxWorks or Linux

CDROM Drive

General

Power Consumption (typ.)  
< 22 W

Warranty  
3 years

Current Requirements (typ.)  
12 V 0.09 A
  5 V 3.63 A
  3.3 V 0.58 A
  -12 V 0.06 A

Front-Panel LEDs indicate module status

Environmental and Physical

Operating Temperature  
0° to 40°C

Required Airflow  
> 2 m/s in situ

Relative Humidity*  
5 to 95% (non-condensing)

Shock*  
30 G, half-sine pulse

Vibration*  
5–500 Hz, random

Safety  
Complies with EN61010-1

EMC Immunity  
Complies with EN61326-1
  Industrial Environment

EMC Emissions  
Complies with EN61326-1 Class A
  for radiated emissions

Dimensions  
6U CompactPCI standard (PXI compliant)
  233 mm x 160 mm x 20 mm

*As defined by MIL-PRF-28800F Class 3

Front panel complies with IEEE1101.10

Certification and Compliance
## Ordering Information

<table>
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<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>TC840</td>
<td>Twelve-channel, wide-range, single-stop Time-to-Digital Converter</td>
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<tr>
<td>TC840-W5</td>
<td>5-year extended warranty</td>
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Items not listed in the current price list may only be available upon specific request. Please contact your local representative for more information.

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For other sales and service representatives around the world, see our website at:  
www.acqiris.com

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ZL010320A/February 2006